Design of a 60W MOS Power Amplifier

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SUMMARY: The power amplifiers in a sound system will be responsible for increasing the input to a certain level at which the speaker can play audio in a space with adequate sound pressure. When these spaces are wide, it takes a lot of pressure and this requires a high power, which should be given to the speaker without causing a variation in the pattern of the input signal. To achieve this goal is mainly used this concept: a suitable configuration, also called topology. The audio power amplifiers are mostly being built under the AB topology, achieving maximum theoretical efficiency of 78.5%. This paper presents an analysis of an MOS power amplifier designed under this topology, showing characteristics, quality measures and indices, resulting in an efficient audio amplifier. This work was realized as open ended problem project.

1 INTRODUCTION

Audio amplifiers were first implemented in 1912 with vacuum tubes, when class A was the only configuration in use, class B was developed time after (in valves as well). From that time until the present, designed topologies have been implemented and have been improved, even more when the transistor was created. Thus we have today topologies: Class A, B, C, AB, D and standardized versions E, G and H. However, most audio power amplifiers that exist currently in the market present AB topology, achieving real efficiency of approximately 60% and a low THD (total harmonic distortion). This configuration is used because it allows the two transistors in the output stage work at the same time for a brief moment to avoid zero crossing distortion. Also, higher performance than Class A can be achieved and a minor distortion than class B.

About the development of our circuit, to get an idea of the choice of components, we considered the parameters related to the power that should be in the load resistance, plus various simulations were made to confirm the correct choice.

Next, we analyzed the overall architecture of the steps our circuit has, especially identifying the reason for each one. This step also helped in the choice of components.

Likewise, much attention was paid to the analysis of THD finishing circuit as this value, being smaller allows components in the circuit and speaker with more precise performance by reducing the harmonics caused by nonlinearity some components.

In this exhibition we will show an audio amplifier, in which we use a design of a power amplifier, which are those that, apart from supplying a higher voltage, also provide a higher current (voltage amplification and current amplification, and thus, power amplifier).

OBJECTIVES:

- The design of an amplifier with a gain of 50 V/V, 8 ohms load, input resistance of 47k, less than 1% THD and a cutoff frequency of 100kHz based on an example circuit and applying re-engineering scheme, finding the different values of elements and parameters that may be included in the development of our work.
- The application of the different aspects to consider, previously seen in class.

2 PRESENTATION OF THE PROBLEM

The operation in class A has the advantage of having a small distortion. While in class B has a higher efficiency. The class AB operation is between these two extremes. The point Q (quiescent) is slightly above the cutoff, so it is found in the lower limit of the linear portion (without distortion) of curves of operation. The transistor then supports a collector current different from zero during a little over 50% of the time.

This open-ended problem gives us a goal to design a power amplifier with MOS transistors 60Wrms output and feedback, plus it must fulfill the following specifications: total gain 50V/V, the load resistance that will be simulating the speaker 8 ohm, input resistance of 47k ohms, the cutoff frequency to 100kHz and the THD should be less than 1%.

What we propose with our circuit (Figure 1) is to achieve or approach these values and what we get after the simulation of it were, roughly, the main results: 60.06W power in the load resistance, the amplifier total gain 50.69V/V and a TDH equal to 0.12%.

The development of the circuit was simulated in the software Multisim V.10 to verify the proper operation and verify the data required. For being a simulation, we are ignoring some considerations to keep in case of an implementation such as the use of protection against short circuit at the output, sinks on mosfets, power of the resistors, etc..

Description of the Circuit

The developed amplifier circuit is in Figure 1 and the list of components is in Table I. The power supply is double (±Vcc), improving the rejection of the ripple power supply and allowing the direct coupling of the load resistance, it means you do not need an electrolytic capacitor coupling between the output - speaker to decrease the DC voltage to zero, the use of dual source already performs this work.

The bandwidth is limited by C1, R1, C2 and R2. The transistors Q1 and Q2 are the first differential stage, the current source is determined by R3. P1 allows better tuning of the DC voltage to the amplifier output.

The input sensitivity is 1.6 volts. Gain 50.69V / V is determined by the ratio R7/R6 and can be modified by varying the R7. The transistors Q5 and Q6 make the second differential stage. The transistors Q3 and Q4 form a current mirror, which makes the second differential stage drain the same amount of current. By doing this we can get more gain and excellent linearity.

The output mosfets work in class AB operating in common source configuration. This gives us an advantage because as the gain is approximately 1, it reduces the oscillation of the value of the output power. Its bias current is determined by multiplying the base-emitter voltage located between the current mirror and the second differential stage, while serving as a compensator due to temperature effects.

Another important aspect of this multiplier is that by varying the temperature causes a variation in the current, and when this happen also varies the collector-emitter voltage, but this must remain in the active region and depends on the base-emitter voltage.

The added capacitor serves as a corrector of capacitive area. More aspects of this section of the circuit will be explained later in the solution itself.

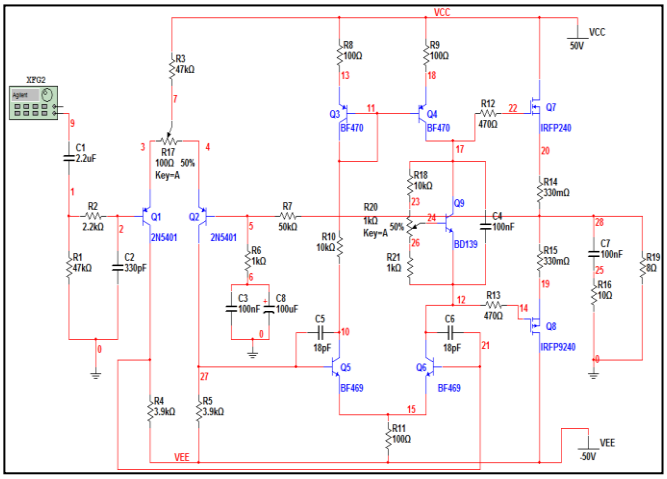


Figure 1. Power amplifier design

Power amplifier input:

The input stage is a differential amplifier using PNP transistors (Q1 and Q2), the polarization resistance (R3) acts as a current source.

The differential amplifier using PNP transistors (Q5 and Q6) has an active load. This active load (Q3 and Q4) acts as a current source with extremely high impedance. Therefore, the voltage gain of the differential amplifier is much greater than before.

Power amplifier output:

The amplified signal coming from the differential amplifier (Q5 and Q6) goes to the final stage, an emitter follower in class B, AB amplifier (Q7 and Q8). Due to the symmetrical feed (equal positive and negative voltages), the output voltage is ideally 0 V when the input voltage is 0. Any deviation from this is called output offset voltage. When there is a Vin with a positive voltage, the Vout will have a positive voltage. So, if voltage Vin is negative, then have a negative voltage Vout. Ideally, Vout can reach + Vcc or -Vee without any signal clipping.

Voltage Regulator:

Crossover distortion of the AB amplifier (Q7 and Q8) is removed by a VGG (Vgate-gate) greater than the sum of Vgs-7 and-8. The voltage VGG is maintained against temperature changes by a pnp transistor (Q9). The capacitor C4 is cut at very high frequencies.

Capacitors:

C1, coupling capacitor which is used for the AC signal to not destabilize the operating point.

C2, decoupling capacitor which causes in very high frequencies, Vin doesn't amplifies.

C3 y C8, coupling capacitors.

C5 and C6, compensation capacitors that increase the bandwidth of the differential amplifier (Q5 and Q6) and make the output more stable.

C4, decoupling capacitor that is cut in very high frequencies.

3 DESCRIPTION OF THE SOLUTION

The following table (Table 1) shows the components used in the design of the amplifier:

Tabla 1

Components List			
C1=2.2uF	R2=2.2kΩ	R14=R15=0.33Ω	Q8=IRFP9240
C2=330pF	R4=R5=3.9kΩ	R16=10Ω	R17=P1=100Ω
C3=C4=100nF	R6=R21=1kΩ	Q1=Q2=2N5401	R20=P2=1kΩ
C8=100uF	R7=50kΩ	Q3=Q4=BF470	R19=R_L=8Ω
C5=C6=18pF	R8=R9=R11=100Ω	Q5=Q6=BF469	-
C7=100nF	R10=R18=10kΩ	Q9=BD139	-
R1=R3=47kΩ	R12=R13=470Ω	Q7=IRFP240	-

Design Criteria:

We propose here a simple design of a MOSFET amplifier using also BJT transistors. The power is + / -60 W at 8 ohms.

Given the simplicity of the circuit, the distortion is +/-0.1%. The bandwidth at 3 db goes from 4 Hz to 96 kHz and is limited by C1, R1, C2 and R2.

Transistors Q1 and Q2 are together a first differential stage, the current source +/-1 mA is provided by R3. If we want to make an improved version, the source of energy could be more effective in stability. We can set a more stable DC value in the first stage using BJTs as a current source.

The input sensitivity should be 1.2 volts. Requested gain of 50 V/V is defined by R7/R6. You can change this value by changing the value of R7.

Transistors Q5 and Q6 form the second differential stage. Transistors Q3 and Q4 work as a current mirror, this forces the second differential stage to drain the same current. So you get a high gain and excellent linearity.

MOSFET output transistors operate in class AB, the quiescent current is set to 50-100 mA by P2 (2.5k potentiometer).

The supply voltage should be between 45 and 55 volts DC (positive and negative).

For setting quiescent current, you must set P2 in minimal resistance, place a multimeter in mV DC range across on R14 or R15 leads, turn slowly the screw until you read a 16,5 mV value, which correspond to a 50 mA quiescent current.

In real applications, we can use 2 fuses. They work as an elementary output short-circuit protection. This will not be included in the design and simulation because we want to keep the simplicity of the circuit.

Another thing that should be kept in mind is the use of a heatsink with a thermal resistance less of 2° C / W. It's highly required in real applications.

More considerations for real applications are: all resistors have to be 1% metal film 1/4 watt. And also, before connecting a speaker at amplifier output, connect a multimeter at output and look on DC output voltage. This level never may be greater than 50 mV. If it is so, check all amplifiers for a mistake. Also, change Q2 with another device and check again.

Calculation

According to data specified in the design

1) Calculating Vo

Assuming the circuit is giving 60W power:

$$P_L = 60Wrms$$
$$R_L = 8\Omega$$

$$60 = \frac{1}{2} \times \frac{{V_O}^2}{R_L} \rightarrow If\ P_L = 60\ W\ \rightarrow\ V_O = 30.98\ V_{peak}$$

The experimental value of Vo is 61.9 Vpp, so divided by 2 we obtain 30.95 V_{peak} which is similar to the theoretical result.

2) Calculating I_L

$$i_L = \frac{30.98\ V}{8\Omega} = 3.873\ A_{peak}$$

3) Calculating I_Q

Assuming the I_Q is the 10% of I_L we obtain:

$$I_Q = 10\%\ de\ i_L \ \rightarrow I_Q = 0{,}387\ A = 387\ mA$$

4) Calculating Vcc

Assuming $V_{ds7} = 16\,V$ to ensure the output signal (Vo) to be out of an apparent distortion when we have Vo and i_L on their peak values (this is only theoretical criteria).

We add the value of the Vout voltage in Vds, plus the voltage in R14 obtaining as a result the value of the voltage sources.

$$\rightarrow V_{cc} = 30.98 + 16 + 3.873 * 0.33 \cong\ 48.26V$$

The power supply must provide 50 volts symmetrically. This theoretical result is nearly as requested.

The theoretical maximum current to be supplied by each source is:

$$I_L = \frac{V_{CC}}{R_L} \qquad (1)$$

$$I_L = \frac{48.26}{8} = 6.03\ A$$

5) To obtain the gain of 50 V/V

R7/R6 with R6 as constant.
Then R7 would be:

R7=1000x50=50kΩ

6) Calculation of Gain and Feedback

To gain, we apply the known relationship of gain for Op-Amps but considering the effective output of the amplifier, which is right after the power amp stage. Then, for any feedback effect the configuration applied can work properly. Finally we apply a feedback to the circuit by using Rb.

$$Av = (1 + \frac{Rb}{Ra}) \qquad (2)$$

This formula is being used because we want our gain to be 50 V/V. And also that Ri is 47k (due to the requirement of the input resistance).

Feedback reduces the crossover to negligible levels. The problem of high frequency oscillation can occur near to crossover points due to poor frequency response near the cutoff region of the transistors (increase phase shift). This problem can be eliminated with a feedback capacitor (C3 and C8 work as feedback compensation).

Then, we find Rb value:

Rb= feedback resistance= 2,3 MΩ

7) Calculation of power and efficiency

In quiescent:

Power extracted from the source Vcc and –Vcc.

The analysis is performed on the stage with MOSFETs IRFP240

$$P_{supply+} = V_{cc} * I_{mos} \qquad (5)$$

With SIGNAL:

For Q7 y Q8:

$$I_{Lmean} = \frac{V_{opeak}}{\pi} * \frac{1}{R_L} \qquad (6)$$

$$P_{supply} = I_{Lmean} * V_{cc} \qquad (7)$$

$$P_{R14} = P_{R15} = I_{Lmean}^2 * R_{14} \qquad (8)$$

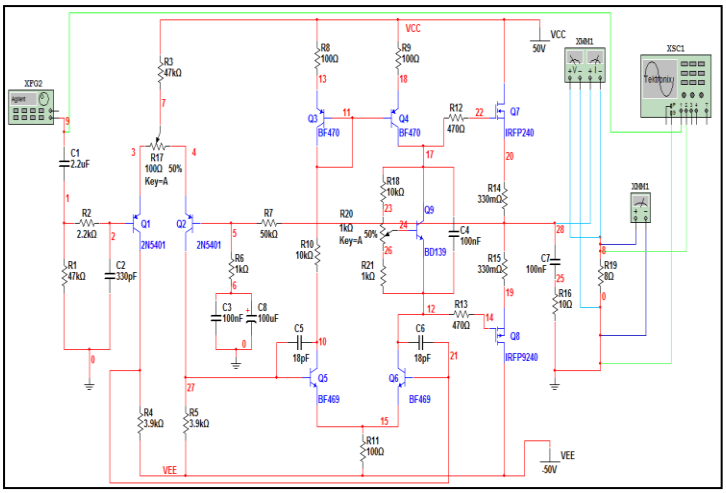
And using eq. (3) we find the power in the load resistance:

P_L=60W

Then,

$$P_{total\ supply} = 2P_{supplyDC} + 2P_{supplyAC} \qquad (9)$$

$$\text{Total efficiency} = \frac{P_L}{P_{Total\ supply}} \qquad (10)$$



4 RESULTS

Figure 2. Measuring points in the circuit

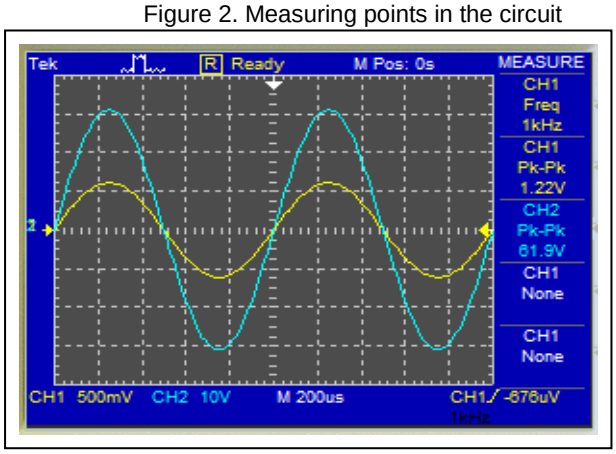


Figure 3. Input (yellow) / output (blue) relation

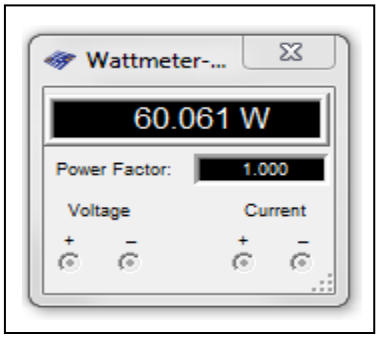


Figure 4. Power in the load resistance

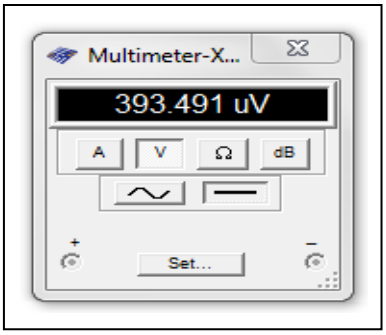


Figure 5. DC voltage in the load resistance

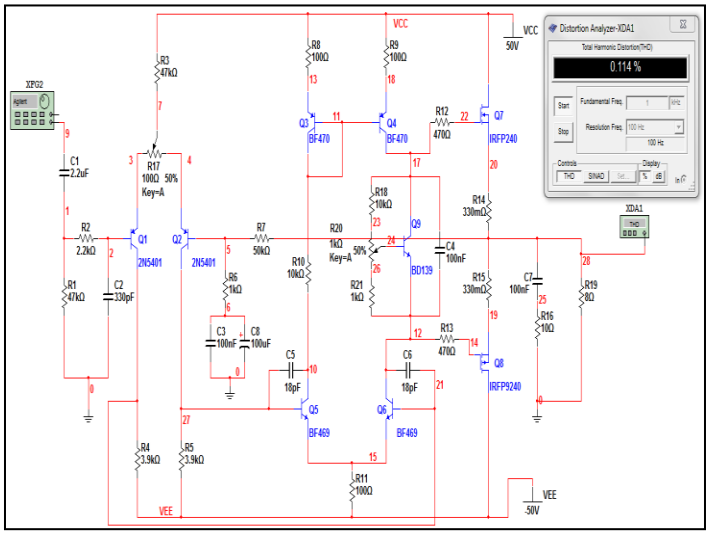
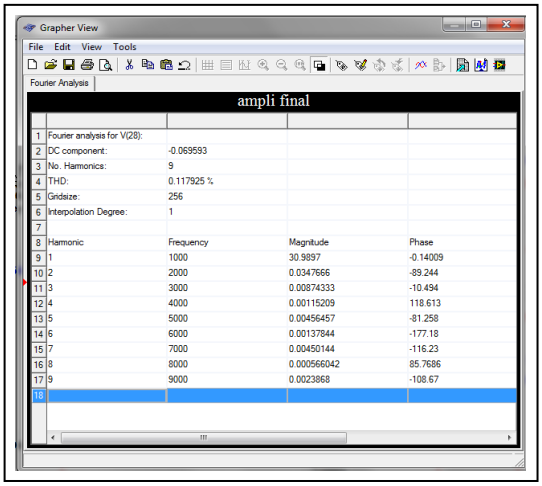


Figure 6. First method to find THD



1	Fourier analysis for V(28):			
2	DC component:	-0.069593		
3	No. Harmonics:	9		
4	THD:	0.117925 %		
5	Gridsize:	256		
6	Interpolation Degree:	1		
7				
8	Harmonic	Frequency	Magnitude	Phase
9	1	1000	30.9897	-0.14009
10	2	2000	0.0347666	-89.244
11	3	3000	0.00874333	-10.494
12	4	4000	0.00115209	118.613
13	5	5000	0.00456457	-81.258
14	6	6000	0.00137844	-177.18
15	7	7000	0.0045014	-116.23
16	8	8000	0.000566042	85.7686
17	9	9000	0.0023868	-108.67
18				

Figure 7. Second method to find THD

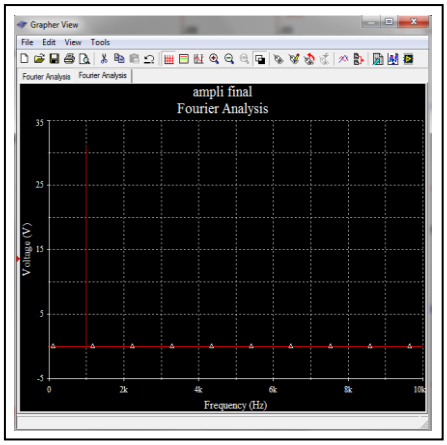


Figure 8. Fourier analysis of the final amplifier

Applications:

- Power amplifiers are essential for many applications, such as radio frequency audio.
- Nowadays, there are a variety of electronics such as televisions, videos, music equipment, digital watches and, of course, computers using power amplifiers.
- Also can be used to implement a distributed speaker system, with the aid of a mixer.
- Sound systems for fixed installations (e.g. shopping malls, airports, etc.) with limited requirements in terms of sound quality, is often used a variation known as Distribution Systems with Constant Voltage (CV).

5 CONCLUSIONS

- The power amplifiers are converters that transform the energy of the source into an output power signal. These can be either class A, B, AB and C, which have different parameters of efficiency and use.
- A power amplifier circuit consists basically of BJT transistors resistors and capacitors. Modifications such as the use of MOSFET seek greater circuit performance and overall tolerance to temperature variations. The purpose of the power amplifier is to provide a maximum output voltage with symmetrical excursion without distortion at a low load resistance.
- Thermal stability problems come to carve completely in these amps because they are handling large powers. This factor should be very important in the design because it has a great influence in the response stability.
- To control the temperature on power components such as the MOSFETs used is necessary to use a Vbe multiplier so that there are no increments in temperature and therefore fluctuations in the output.
- In case of implementation, we must adhere sinks, fans (which can be placed in the case of a pc) and fuses to ensure that there is no overheating and/or a short circuit.
- We should also consider installing a low-pass filter on each entry line to avoid problems of high frequency oscillations at the output.

6 BIBLIOGRAPHY

[1]http://www.forosdeelectronica.com/f31/amplificador-mosfet-100w-rms-5222/

[2]http://www.forosdeelectronica.com/f31/calculo-amplificador-clase-ab-6911/

[3]http://www.worldlingo.com/ma/enwiki/es/Electronic_amplifier

[4]http://www.unicrom.com/topic.asp?TOPIC_ID=6060&FORUM_ID=2&CAT_ID=2&Forum_Title=Amplificadores&Topic_Title=Amplificador+de+clase+AB

[5]http://www.pcpaudio.com/pcpfiles/doc_amplificadores/etapas_salida/etapas_salida.html#AB

[6]http://electronicacompleta.com/lecciones/amplificador-de-potencia-de-audio/

[7]http://www.taringa.net/posts/info/1162187/Acerca-del-Audio_-Watts-PMPO-y-RMS.html

[8]http://www.rocketroberts.com/techart/powerart_a.htm

[9]Adel Sedra y Kenneth Smith, "*Circuitos Microelectrónicos*", 4ta ed., Oxford University Press, US, 1998

[10]Albert P. Malvino, *"Principios de Electrónica"*, 6ta ed., McGraw-Hill, Mx, 2000

[11]Andrew Singmin, *"Practical Audio Amplifier Circuit Project"*, ed. única, Newnes, US, 2000

[12]Rudolf F. Graf, *"Amplifier Circuits"*, ed. única, Newness, US, 1996